Claims

I claim:

1. An array of electromechanical micromirror devices comprising a plurality of electromechanical micromirror devices disposed in a 1-dimensional or 2-dimensional array, comprising:

a device substrate with a 1st surface and a 2nd surface;

control circuitry disposed on said 1st surface of said substrate; and

an array of micromirror sections disposed on said 2nd surface of said substrate, wherein each said micromirror section comprises:

a micromirror whose reflective surface is substantially planar when said micromirror is in its undeflected state, with neither recesses nor protrusions; and

at least 1 support structure for supporting said micromirror.

2. The array of claim 1, wherein said control circuitry is selected from the group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar transistor circuits, BiCMOS circuits, DMOS circuits, HEMT circuits, amorphous silicon thin film transistor circuits, polysilicon thin film transistor circuits, SiGe transistor circuits, SiC transistor circuits, GaN transistor circuits, GaAs transistor circuits, InP transistor circuits, CdSe transistor circuits, organic transistor circuits, and conjugated polymer transistor circuits.

3. The array of claim 1, wherein said device substrate is selected from the group consisting of silicon-on-insulator (SOI), silicon, polycrystalline silicon, glass, plastic, ceramic, germanium, SiGe, SiC, sapphire, quartz, GaAs, and InP.

4. The array of claim 1, wherein each said micromirror section additionally comprises at least 1 addressing electrode for actuating said micromirror.

5. The array of claim 4, additionally comprising at least 1 electrically conductive routing line integral with said device substrate that connects said control circuitry to said at least 1 addressing electrode of at least 1 of said micromirror sections.

6. The array of claim 5, wherein said at least 1 electrically conductive routing line comprises a via through said substrate and a metallization in said via.

7. The array of claim 1, wherein said device substrate additionally comprises an insulating layer between said 1st surface and said 2nd surface.

8. The array of claim 1, wherein said micromirror is a metallic mirror.

9. The array of claim 1, wherein said micromirror is a multilayer dielectric mirror.

10. The array of claim 1, wherein the reflectivity of the reflective side of said micromirror is at least 80 %.

11. The array of claim 10, wherein said reflectivity is at least 90 %.

12. The array of claim 11, wherein said reflectivity is at least 95 %.

13. The array of claim 1, wherein the reflective surface of said micromirror has no edges that are perpendicular to the projection of the incident light propagation vector onto the plane of said device substrate.

14. The array of claim 1, wherein the reflective surface of said micromirror, when said micromirror is in its undeflected or deflected states, has at least 1 edge that is greater than 60 degrees and less than 120 degrees from the projection of the incident light propagation vector onto the plane of said device substrate, and wherein said at least 1 edge is covered by a layer of light absorbing material.

15. The array of claim 1, wherein said micromirror is in the shape of a polygon.

16. The array of claim 15, wherein said polygon is selected from the group consisting of a rectangle and a hexagon.

17. The array of claim 1, wherein said micromirror section additionally comprises:

a torsion hinge that is disposed to support said micromirror support structure; and

a pair of support structures for said torsion hinge that supports said torsion hinge on said substrate.

18. The array of claim 1, wherein said micromirror section additionally comprises at least 1 stopping member that limits the rotation of said micromirror.

19. The array of claim 18, wherein said at least 1 stopping member comprises:

a 1st stopping member that limits the rotation of said micromirror in a 1st direction; and

a 2nd stopping member that limits the rotation of said micromirror in a direction opposite to said 1st direction.

20. A spatial light modulator (SLM) comprising an array according to claim 1.

21. A method of fabricating an array of electromechanical micromirror devices, comprising the steps of:

providing a device substrate with a 1st surface and a 2nd surface;

forming control circuitry on said 1st surface of said substrate; and

forming a plurality of micromirror sections on said 2nd surface of said substrate, comprising the steps of:

forming a plurality of support structures for supporting micromirrors; and

forming a plurality of micromirrors such that each micromirror has a reflective surface that is substantially planar when said micromirror is in its undeflected state, with neither recesses nor protrusions.

22. The method of claim 21, wherein said step of forming control circuitry comprises a step of fabricating circuits selected from the group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar transistor circuits, BiCMOS circuits, DMOS circuits, HEMT circuits, amorphous silicon thin film transistor circuits, polysilicon thin film transistor circuits, SiGe transistor circuits, SiC transistor circuits, GaN transistor circuits, GaAs transistor circuits, InP transistor circuits, CdSe transistor circuits, organic transistor circuits, and conjugated polymer transistor circuits.

23. The method of claim 21, wherein said device substrate is selected from the group consisting of silicon-on-insulator (SOI), silicon, polycrystalline silicon, glass, plastic, ceramic, germanium, SiGe, SiC, sapphire, quartz, GaAs, and InP.

24. The method of claim 21, wherein said step of forming said micromirror sections additionally comprises a step of forming a plurality of addressing electrodes for actuating said plurality of micromirrors.

25. The method of claim 24, additionally comprising a step of forming a plurality of electrically conductive routing lines integral with said device substrate that connects said control circuitry to said plurality of addressing electrodes.

26. The method of claim 25, wherein said step of forming said plurality of electrically conductive routing lines comprises the steps of:

forming at least 1 via through said substrate; and

forming a metallization in said at least 1 via.

27. The method of claim 21, wherein said device substrate additionally comprises an insulating layer disposed between said 1st surface and said 2nd surface.

28. The method of claim 21, wherein said step of forming micromirrors comprises a step of forming a reflective metallic coating.

29. The method of claim 21, wherein said step of forming micromirrors comprises the steps of forming a reflective multilayer dielectric coating.

30. The method of claim 21, wherein said step of forming micromirror sections comprises the steps of:

forming said plurality of micromirror support structures such that it is embedded in a layer of sacrificial material;

planarizing said sacrificial layer such that said sacrificial layer and the top of said micromirror support structures are substantially planar;

depositing a micromirror material on said planar surface;

patterning said micromirror material to form a plurality of micromirrors; and

removing said sacrificial layer by an etching process.

31. The method of claim 30, wherein said sacrificial layer material is selected from the group consisting of photoresist polymer, silicon oxide, silicon nitride, silicon oxynitride, and amorphous silicon.

32. The method of claim 30, wherein said planarizing step comprises a chemical mechanical polishing (CMP) process.

33. The method of claim 21, wherein said step of forming a plurality of micromirrors comprises a step of:

patterning each micromirror such that its reflective surface has no edges that are perpendicular to the projection of the incident light propagation vector onto the plane of said device substrate.

34. The method of claim 21, wherein said step of forming a plurality of micromirrors comprises the steps of:

patterning each micromirror such that its reflective surface, when said micromirror is in its undeflected or deflected states, has at least 1 edge that is greater than 60 degrees and less than 120 degrees from the projection of the incident light propagation vector onto the plane of said device substrate; and

covering said at least 1 edge with a layer of light absorbing material.

35. The method of claim 21, wherein each said micromirror is patterned to be in the shape of a polygon.

36. The method of claim 35, wherein said polygon is selected from the group consisting of a rectangle and a hexagon.

37. The method of claim 21, additionally comprising a step of forming a torsion hinge for supporting each said micromirror support structure, said step comprising:

forming a plurality of support structures for supporting torsion hinges; and

forming a plurality of torsion hinges.

38. The method of claim 21, additionally comprising the step of:

forming at least 1 stopping member that limits the rotation of each said micromirror.

39. The method of claim 38, wherein said step of forming at least 1 stopping member comprises:

forming a 1st stopping member that limits the rotation of each said micromirror in a 1st direction; and

forming a 2nd stopping member that limits the rotation of each said micromirror in a direction opposite to said 1st direction.

40. A method of fabricating an array of electromechanical micromirror devices, comprising the steps of:

providing a silicon-on-insulator substrate with an epitaxial top silicon layer, an insulator layer, and a bottom silicon layer;

forming control circuitry on said epitaxial top silicon layer;

removing said bottom silicon layer, thereby exposing the insulator layer; and

forming a plurality of micromirror sections on said exposed insulator layer, comprising the steps of:

forming a plurality of support structures for supporting micromirrors; and

forming a plurality of micromirrors whose reflective surface is substantially optically flat when said micromirror is in its undeflected state, with neither recesses nor protrusions.

41. The method of claim 40, wherein said step of forming control circuitry comprises a step of fabricating circuits selected from the group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar transistor circuits, BiCMOS circuits, and DMOS circuits.

42. The method of claim 40, wherein said step of removing said bottom silicon layer comprises backgrinding.

43. The method of claim 40, wherein said step of removing said bottom silicon layer comprises chemical mechanical polishing (CMP).

44. The method of claim 40, wherein said step of forming said micromirror section additionally comprises a step of forming a plurality of addressing electrodes for actuating said plurality of micromirrors.

45. The method of claim 44, additionally comprising a step of forming a plurality of electrically conductive routing lines integral with said device substrate that connects said control circuitry to said plurality of addressing electrodes.

46. The method of claim 45, wherein said step of forming said plurality of electrically conductive routing lines comprises the steps of:

forming at least 1 via through said substrate; and

forming a metallization in said at least 1 via.

47. The method of claim 40, wherein said step of forming micromirror sections comprises the steps of:

forming said plurality of micromirror support structures such that it is embedded in a layer of sacrificial material;

planarizing said sacrificial layer such that said sacrificial layer and the top of said micromirror support structures are substantially planar;

depositing a micromirror material on said planar surface;

patterning said micromirror material to form a plurality of micromirrors; and

removing said sacrificial layer by an etching process.

48. The method of claim 47, wherein said planarizing step comprises the chemical mechanical polishing (CMP) process.